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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,756	04/15/2004	Jeffrey Orion Pritchard	ALTRP110/A1238	1217

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EXAMINER	
SIEK, VUTHE	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,756	PRITCHARD, JEFFREY ORION	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/13/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/826,756 filed on 4/15/2004. Claims 1-26 remain pending in the application.

Specification

2. In the specification, page 17, line 20, "voltage can information is provided" should be changed to –voltage information is provided--. Correction is requested.

Claim Objections

3. Claims 1, 3, 10, 12, 19 and 21 are objected to because of the following informalities: claim 1, "the programmable chip" should be changed to –the programmable chip system--, in lines 6 and 7; claim 10, line 1 "a programmable device" should be changed to –a programmable chip system", in order to provide the same invention as in claims 1 and 19; claim 10 line 8; "programmable chip" should be changed to –programmable chip system—to provide proper claim antecedent as suggested; claim 19, line 8, "programmable chip" should be changed to –programmable chip system--; claims 3, 12 and 21, lines 1 & 2, "ground pints" should be changed to –ground pins--, to correct informality. Appropriate correction is required. Note that Examiner has examined the claims as above suggested changes.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 4-11, 13-20 and 22-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Zeidman et al. (US 2005/0010378 A1).

6. As to claims 1, 10 and 19, Zeidman et al. teach a method/system/apparatus for implementing a programmable chip system (see summary, Fig. 1-9), the method comprising receiving customization information associated with a processor core (Fig. 3, numerous processor cores) and a plurality of programmable chip components (Fig. 1, numerous devices); configuring the processor core and the plurality of programmable chip components for implementation on the programmable chip (Fig. 7, user takes customization information to create a target system 703 on a printed circuit board); determining voltage and ground pins associated with the programmable chip [system] (at least see 0017, 0029-0030, where the reference teaches the resulting netlist created by a is input to a layout program from a third party that can produce a layout for a printed circuit board (PCB); the system tools as taught by the reference includes schematic capture tools, netlist tools, layout tools, fabrication tools and assembly tools are used to create a physical layout of programmable chip system on a printed circuit board. The netlist describes connectivity between the selected processor core and custom devices, where the tools described above are use to create a physical layout of the programmable chip system on the board. Since the processor core and custom devices used powers, the specification file of the processor core and custom devices

must inherently include power and ground pins that must be determined for connection between the processor core and custom devices and to off-chip components; note that power/ground pins information is described in Chung et al. US 2002/00833400 A1 (0034, 0039; see also 7,117,459 and 7,120,885 for power and ground pins used for connection) for illustration that pins information must be included for connectivity by layout tools); providing a netlist, wherein a printed circuit board layout tool uses the netlist to generate a layout coupling the processor core and the plurality of programmable chip components to off-chip components (at least see 0029-0030, see above rejection; the programmable chip system as taught by Zeidman is used for a UART).

7. As to claims 2, 11 and 20, Zeidman et al. teach the netlist created is a printer circuit board netlist (at least see 0029-0030).

8. As to clams 4, 13 and 22, Zeidman et al. teach, wherein the plurality of programmable chip components are received from a library (at least see 0002).

9. As to clams 5, 14 and 23, Zeidman et al. teach, wherein customization information includes parameterization information (at least see 0002-004, 0018-0020).

10. As to claims 6, 15 and 24, Zeidman et al. teach, wherein the processor core and the plurality of programmable chip components are connected using a simultaneously multiple primary component fabric (at least see 0019-0030).

11. As to claims 7-8, 16-17 and 25-26, Zeidman et al. teach, wherein the off-chip component is an external memory device and an application specific standard product (at least see 0002—004, 0018-0019).

12. As to claims 9, 18, Zeidman et al. teach, wherein the printed circuit board layout tool takes the netlist and generates schematic traces (at least see 0017, 0029-0030).

13. Claims 1-2, 4-11, 13-20 and 22-26 are rejected under 35 U.S.C. 102(e) as being anticipated Pritchard et al. (7,149,827 B1).

14. As to claims 1, 10 and 19, Pritchard et al. teach substantially the same claimed invention of a method/system/apparatus for interconnecting on-chip components (processor core and programmable devices with customization information for the on-chip system configuration) with off-chip components through various of buses, fabrics, and input/output lines. Note that the each of components for connection must used power and ground lines, therefore a determination of ground and power pins must be inherently included for connection by layout tools (see Fig. 1-9, Fig. 1 a programmable chip system; Fig. 3 a system connectivity; Fig. 4-6 show examples of a layout connectivity representation of a programmable chip system implemented on a printed circuit board; Fig. 7-8 describes implementation of a programmable chip system; Fig. 9 show a system used to implement the programmable chip implemented on a printed circuit boad).

15. As to claims 2, 4-9, 11, 13-18, 20 and 22-26, Fig. 4-6 show a netlist of a printed circuit board used for layout tools for interconnecting of a processor core and programmable components received from a library with off-chip components that include an external memory device and an application specific standard product.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 3, 12 and 21 are rejected under 35 U.S.C. 103(a) as being obvious over Zeidman et al. (US 2005/0010378 A1) in view of Nakayama et al. (7,120,885 B2) or Tanimoto et al. (7,117,459 B2).

18. As to claims 3, 12 and 21, Zeidman et al. do not teach wherein capacitors are bypassed for ground pins and voltage pins. Nakayama et al. teach that limitation to effectively reduce noise (at least see Fig. 42, 44, at least see col. 12 lines 35-53). Tanimoto et al. also teach that limitation in order to enable bypass capacitors on the PCB to function effectively (at least see Fig. 2, field of the invention, summary). With these motivations, it would have been obvious to practitioners in the art to have capacitors being bypassed for ground pins and voltages pins.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER